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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,537	04/14/2004	Hsien-Yueh Hsu	4443-0111PUS1	4436

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EXAMINER	
TRAN, VINCENT HUY	
ART UNIT	PAPER NUMBER
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/30/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 01/30/2007.

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mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/823,537	HSU, HSIEN-YUEH	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 10/25/06

2. Claims 1-13 are pending for examination.

3. The text of those sections of Title 35, U.S. code not included in this action can be found in a prior Office action.

Response to Arguments

4. Applicant's arguments filed 10/25/06 have been fully considered but they are not persuasive.

Applicant has argued that the present invention can optimizing the performance more efficiently and precisely than Iwazaki, because a plurality of the performance monitor means are applied to connected separately to the corresponding one of bus lines to connect devices because Iwazaki's system only divided to two types, one is the CPU, the other is the peripheral processing unit and devices are regarded as an individual relative to the CPU such that they cannot be monitored or adjusted separately.

Examiner respectfully disagrees with this narrow interpretation of the Iwazaki's system.

The system of Iwazaki may only shows a CPU connected to two peripheral processing unit 31 and 32 by bus 5; however, what Iwazaki specifically teaches is a system that capable of monitoring and dynamically adjusting the operating rate separately for each individual

processing units in according to the flow rate of data transferred in bus line 5 independent of the processing load state of the CPU[1] [col. 2 lines 55-61; col. 3 lines 48-61].

Therefore, for a convention motherboard with multiple buses and wherein each bus comprising of PCI, AGP, RAM, CPU bus line that connected to multiple processing units; it is obvious to one of ordinary skill in the art that, by adapting the method taught by Iwazaki, one would able to optimizing the performance of a computer system by providing multiple monitors to monitor the flow rate on each bus to efficiently and dynamically adjusting the operating rate of each device connected thereto.

Note: It is unclear to Examiner that the argument filed on 10/25/06 is in respond to claim 10 since the limitation in claim 10 is different from claim 1 and 7 since it does not specifically claim a plurality of monitor means connected to respective bus line only that it monitors the flow rate of data of selected device and adjusts the operating rate of the selected device which is anticipated by Iwazaki.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

[1] It is obvious to one of ordinary skill in the art that the two processing units inherently also connected to other processing units beside the CPU. Therefore, the two peripheral processing units 31 and 32 cannot be said to be depended only to the CPU since each is individual being control in according only to the flow rate of data transferred on the bus line connected thereto and not by the processing load of the CPU.

6. Claims 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwazaki.

7. As per claim 10, Iwazaki teaches a method for adjusting the system performance of a computer, for monitoring the actual data flow rates of devices fabricated on a motherboard and adjusting the operating rates of said devices, said method comprising the steps of:

(1) executing a program to make one selected said device be in an operating state [inherent];

(2) measuring a flow rate of data of said selected device in said operating state [col. 6 lines 53-59];

(3) defining a predetermined flow rate of said selected device according to said flow rate of data measured in said step (2) to indicate said selected device is in a busy state [NUM1, NUM2 - From col. 6 line 59 to col. 7 line 13];

repeating said steps (1).about.(3) to define the predetermined flow rates of said devices fabricated on said motherboard [col. 7 lines 9-13];

measuring actual data flow rates of said devices on said motherboard; when said actual data flow rate of one said device exceeds said predetermined flow rate thereof, promoting an operating rate of said device [fig. 3] ; and

when said actual data flow rate of said device is less than said predetermined flow rate thereof, reducing the operating rate of said device [fig. 3; col. 7 lines 25-31].

8. As per claim 11, Iwazaki teaches said flow rate of data is the number of times of accessing data passing through said device per unit time [2C, 2E fig. 2].

9. As per claim 12, Iwazaki teaches said flow rate of data is the number of times of transferring commands through said device per unit time [2D fig. 2].

10. As per claim 13, Iwazaki inherently teaches devices connected to said performance control chip comprise a CPU [2 fig. 5], a north bridge chip, a south bridge chip, an AGP slot, PCI slots and a motherboard power supply.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

13. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Velasco et al. U.S. Patent No. 6,813,674 ("Velasco") in view of Iwazaki.

14. As per claim 1, Velasco teaches an apparatus for adjusting the system performance of a computer, fabricated on a motherboard, said apparatus comprising:

a plurality of performance monitor means [54a...n fig. 2-3 and 50a...n fig. 3], connected respectively to bus line [72, 71, 73 fig. 3; bus from External Request 58a...n; 202, ISA, 229 bus fig. 20] which are connected with devices [52a...n fig. 2-3; 209...228 fig. 20] mounted on the

motherboard, for monitoring the operating state of each device according to the activity of data transferred in the bus lines [col. 8 lines 13-27; col. 9 lines 47- 65; col. 19 lines 10-41]; and

a performance control chip [53a...n fig. 3], connected separately to the devices, for adjusting the operating rate of the devices responsive to the performance monitor means, said performance control chip being capable of ascertaining the operating state of each device is busy or not, so as to increasing or decreasing the operating rate of the device [from col. 9 lines 59 to col. 10 lines 22].

Velasco does not teach the performance monitor means for monitoring the operating state of each device according to the flow rate of data transferred in the bus lines.

Iwazaki teaches another apparatus directed to a clock control type information processing apparatus for dynamically adjusting the clock signals supplied by a performance control mean according to the load state of devices. Specifically Iwazaki teaches

a performance monitor means [44 fig. 5], connected respectively to a bus line [5 fig. 5] which are connected with devices [2, 31, 34 fig. 5] mounted on said motherboard, for monitoring the operating state of each said device according to the flow rate of data transferred in said bus lines[S401 fig. 3; col. 6 lines 34-37, 53-59]; and

a performance control chip [41 fig. 5], connected separately to said devices, for adjusting the operating rate of said devices responsive to said performance monitor means, said performance control chip being capable of ascertaining the operating state of each said device is busy or not, so as to increasing or decreasing the operating rate of said device [From col. 6 line 59 to col. 7 line 13; col. 7 lines 25-31; col. 8 lines 52-65].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the apparatus of Velasco with the feature discussed above as taught by Iwazaki.

The motivation for doing so would have been to allow the system the ability to precisely adjusting the clock of the devices in response to the load states of the bus which is more efficient since Velasco's devices could operate only in either normal mode or power saving mode.

15. As per claim 2, Velasco teach the bus lines comprise: a PCI bus line, connected between a south bridge chip and a PCI slot; an AGP bus line, connected between a north bridge chip and an AGP slot; a RAM bus line, connected between said north bridge chip and a RAM device; and a CPU bus line, connected between a CPU and said north bridge chip [fig. 20].

16. As per claim 3, Velasco inherently teaches devices connected to said performance control chip comprise a CPU [fig. 20], a north bridge chip, a south bridge chip, an AGP slot, PCI slots and a motherboard power supply.

17. As per claim 4, Iwazaki inherently teaches performance monitor means comprises a counter, for measuring the number of times of transferring commands or accessing data through one selected said bus line per unit time [col. 6 lines 53-65].

18. As per claim 5, Iwazaki inherently teaches performance control chip comprises: a register, for storing predetermined flow rates of said devices; a comparator, for comparing actual

flow rates provided by said performance monitor means with said predetermined flow rates stored in said register, when said actual flow rate of one selected said device exceeds said predetermined flow rate thereof, said device is ascertained to be busy [col. 6 lines 53-65].

19. Claims 1-5, 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwazaki.

20. As per claim 1, Iwazaki teaches an apparatus for adjusting the system performance of a computer, fabricated on a motherboard, said apparatus comprising:

a performance monitor means [44 fig. 5], connected respectively to a bus line [5 fig. 5] which are connected with devices [2, 31, 34 fig. 5] mounted on said motherboard, for monitoring the operating state of each said device according to the flow rate of data transferred in said bus lines[S401 fig. 3; col. 6 lines 34-37, 53-59]; and

a performance control chip [41 fig. 5], connected separately to said devices, for adjusting the operating rate of said devices responsive to said performance monitor means, said performance control chip being capable of ascertaining the operating state of each said device is busy or not, so as to increasing or decreasing the operating rate of said device [From col. 6 line 59 to col. 7 line 13; col. 7 lines 25-31; col. 8 lines 52-65].

In conclusion, Iwazaki only teaches a generic method for dynamically supplying clock signals to the processing unit and the peripheral devices in response to the flow rate of data transferred in a bus line.

Although not explicitly taught in Iwazaki, the used of a plurality of performance monitor means to connect respectively to different part of the system is an old and well know technique in the art. The examiner takes official notice that these are merely a conventional

method/design-consideration for monitor system performance/operating-state which is commonplace in hardware design. One of ordinary skill in the art would be motivated to modified the system of Iwazaki with the multiple monitor means since not all devices in a computer system would be connecting to one bus line. Therefore, it is obvious to one of ordinary skill in the art to utilize separate monitor means on different bus lines to monitor the operating state of each device which connected thereto.

21. As per claim 2, Iwazaki does not teach the bus lines comprise: a PCI bus line, connected between a south bridge chip and a PCI slot; an AGP bus line, connected between a north bridge chip and an AGP slot; a RAM bus line, connected between said north bridge chip and a RAM device; and a CPU bus line, connected between a CPU and said north bridge chip. However, it is obvious to one of ordinary skill in the art that the generic bus line of Iwazaki encompasses the specific claimed bus lines since the special bus lines do not alter the performance of Iwazaki system.

22. As per claim 3, Iwazaki inherently teaches devices connected to said performance control chip comprise a CPU [2 fig. 5], a north bridge chip, a south bridge chip, an AGP slot, PCI slots and a motherboard power supply.

23. As per claim 4, Iwazaki inherently teaches performance monitor means comprises a counter, for measuring the number of times of transferring commands or accessing data through one selected said bus line per unit time [col. 6 lines 53-65].

24. As per claim 5, Iwazaki inherently teaches performance control chip comprises: a register, for storing predetermined flow rates of said devices; a comparator, for comparing actual flow rates provided by said performance monitor means with said predetermined flow rates stored in said register, when said actual flow rate of one selected said device exceeds said predetermined flow rate thereof, said device is ascertained to be busy [col. 6 lines 53-65].

25. As per claim 7, Iwazaki teaches an apparatus for adjusting the system performance of a computer, fabricated on a motherboard, said apparatus comprising:

a counters [inherent], coupled respectively to the corresponding one of bus lines which are connected with devices, for measuring the flow rate of data transferred in each said bus line per unit time [fig. 2A-2F; col. 6 lines 53-59]; and

a performance control chip [43 fig. 7], connected separately to said devices, being capable of ascertaining each said device is busy or not, so as to increasing or decreasing the operating rate of said device [col. 7 lines 25-31], said performance control chip comprising

a register [inherent], for storing predetermined flow rates [NUM1, NUM2 fig. 3]of said devices;

a comparator [inherent], for comparing actual flow rates measured by said counter with said predetermined flow rate stored in said register [S402, S404 fig. 3], when said actual flow rate of one said device exceeds said predetermined flow rate thereof, said device is ascertained to be busy [abs].

Iwazaki does not teach a plurality of counters [measuring circuit] in which each is coupled to a different bus lines. Iwazaki merely teaches a generic system comprising a counter coupled to a specific bus line to measure the flow rate thereto. The examiner takes official notice that these are merely a conventional method/design-consideration for monitoring different part of a system for performance/operating-state which is commonplace in hardware design. One of ordinary skill in the art would be motivated to modified the system of Iwazaki with the multiple counters since not all devices in a computer system would be connecting to one bus line. Therefore, it is obvious to one of ordinary skill in the art to utilize separate counter on different bus lines to monitor the operating state of each device which connected thereto.

26. As per claim 8 and 9, see discussion in claim 2 and 3.

27. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwazaki as applied to claim 1 above, and further in view of O'Brien.

28. As per claim 6, Iwazaki does not teach the performance control chip is connected to a motherboard power supply on said motherboard and is capable of controlling said operating rate of each said device by adjusting the power supplied thereto.

O'Brien teaches another computer system comprising a activity monitor connected directly to various control bus lines associated with the microprocessor and peripheral devices wherein, depending upon the detected activities, the performance control chip [202 fig. 1] responsively power down selected circuit portions, reduce the frequencies of selected clock signal [col. 1 lines 45-56]. Specifically, O'Brien teaches the performance control chip is

connected to a motherboard power supply [262 fig. 1] on said motherboard and is capable of controlling said operating rate of each said device by adjusting the power supplied thereto [col. 6 lines 40-46; col. 7 lines 8-12].

At time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Iwazaki with the adjusting of the power supplied to control the operating rate of each device of O'Brien in order to further conserve power.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Tran.